High-Speed GaAs SDFL Divider Circuit

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Abstract—**High-speed divider circuits find numerous applications in prescalers for counters, frequency synthesizers, and digital phase locked loops. To accommodate these applications, a high-speed multimode divider circuit has been designed, fabricated, and tested. This circuit, fabricated on semi-insulating Gallium Arsenide substrates, and utilizing Schottky diode FET logic (SDFL) technology, has been tested at a maximum clock frequency of 1.84 GHz. High yields of circuits operating over 1 GHz have been obtained over a number of wafers.**

I. Introduction

THE FIELD OF high-speed GaAs digital integrated circuits is expanding very rapidly [1]. With speeds well into the gigahertz domain [2], and processing capabilities reaching large-scale integration [3], the technology is becoming very attractive, and applications are being sought. Communications is a field where relatively simple high-speed components can impact the performance of full systems. Multimodule high-speed frequency divider circuits, for example, can find numerous applications in prescalers for counters, frequency synthesizers, and digital phase lock loops. To satisfy such applications, a variable module divider capable of eight different operating modes (divide-by-5, -6, -10, -12, -40, -41, -80, and -82) has been designed, fabricated, and tested.

The approach chosen was to use a well-established planar fabrication process, and a well-demonstrated design concept, so that high yields could be obtained. This paper contains a description of the circuit starting from its building blocks. This is followed by a description of the tests performed on wafer and on packaged devices, including automatic high-speed measurements for yield data acquisition. Finally, the yield of high-speed circuits is discussed.

II. Circuit Technology

The fabrication process chosen for the variable modulo divider is the same process which was used for the first demonstration of a large-scale GaAs integrated circuit [3]. This fabrication process has been discussed in detail elsewhere [4]. It is a planar process which features multiple localized ion implantations directly into semi-insulating GaAs substrates. The unimplanted areas provide electrical isolation between circuit elements. The process is relatively simple, requiring only six masks for fabrication. Various sizes of depletion-mode MESFET's with 1-μm gate lengths, along with switching and level shifting diodes are used.

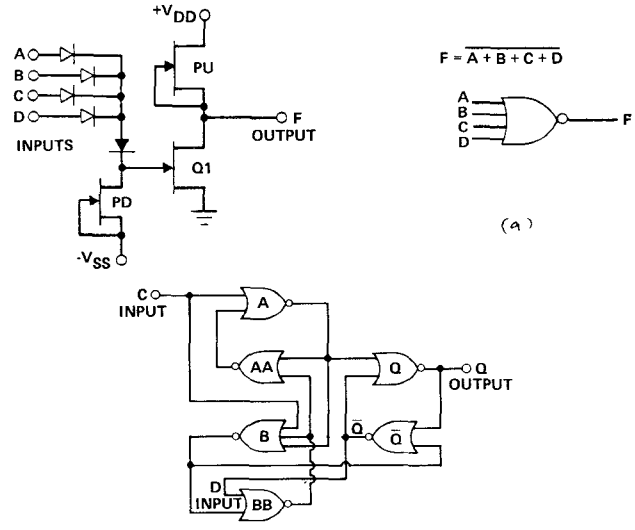

Fig. 1. Building blocks for the variable modulo divider circuit. (a) Schematic of a SDFL NOR gate. (b) Logic diagram of a *D*-type flip–flop with a maximum toggle rate of $1/5\tau_D$.

The approach used to realize this circuit was Schottky diode FET logic (SDFL) [5]. Fig. 1(a) depicts a standard SDFL NOR gate. The switching diodes are connected together to perform the OR function. The level-shifting diode and the small pull-down transistor provide the proper bias to switching transistor $Q1$. This transistor performs the inversion function. The pull-up transistor sources current to subsequent NOR gates when $Q1$ is turned off [6].

Fig. 1(b) shows how the NOR gates are connected to form a *D*-type flip–flop, which is the basic building block of the divider circuit [2]. This particular configuration of flip–flop will operate at a maximum frequency of $1/5\tau_d$ where τ_d is the propagation delay through a single NOR gate. This delay is on the order of 100-ps per gate for our technology employing 1-μm long FET gates.

There are other configurations of flip–flops [7], which have theoretical maximum operating frequencies of $1/2\tau_d'$ where τ_d' is the propagation delay through an OR/NAND gate, and thus can operate faster than the configuration used [8]. However, this faster configuration requires complementary clock inputs, which must be provided by a complementary clock generator. This must be placed on the chip for most practical circuit applications. The faster

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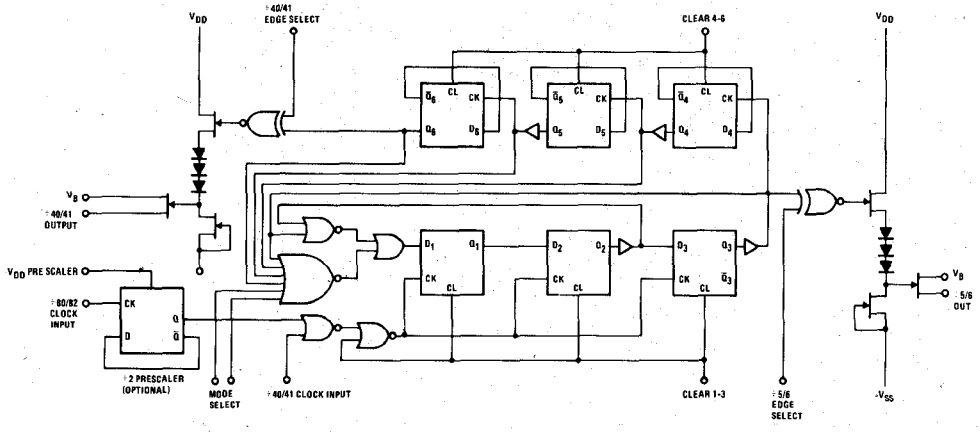

Fig. 2. Schematic of the multimode SDFL divider circuit capable of frequency division by 5, 6, 10, 12, 40, 41, 80, and 82. 80/82 is negative edge triggered input. 40/41 is positive edge triggered input.

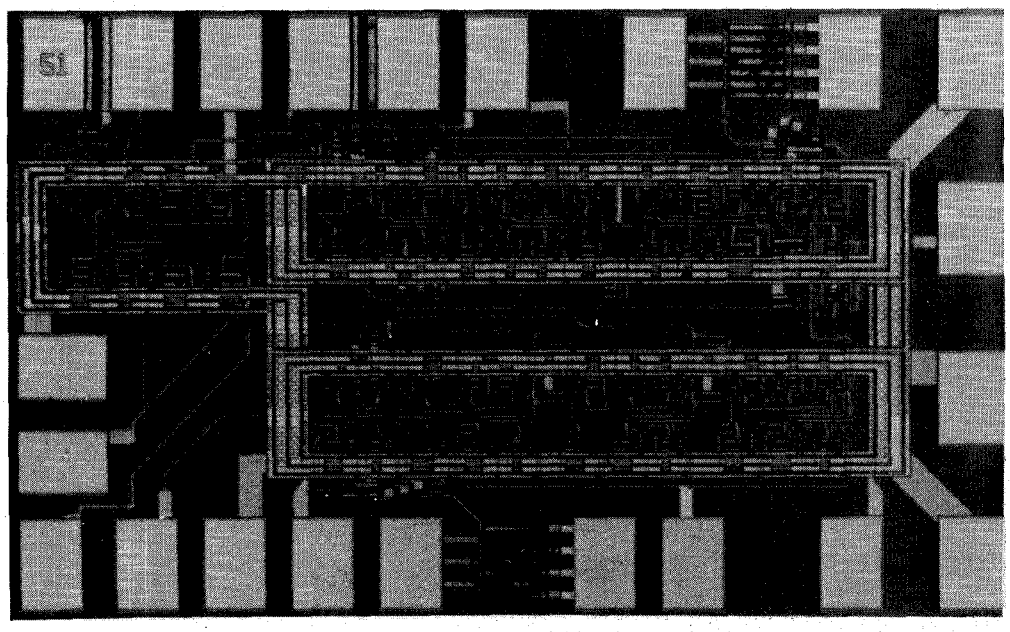

Fig. 3. Photomicrograph of the multimode SDFL divider circuit. The chip size is 1.35×0.9 mm.

flip–flop would also require multilevel logic. This is not a serious obstacle because multilevel logic can be implemented with SDFL [9] or other circuit approaches [7], but some penalty, in terms of complexity and propagation delay per gate is involved ($\tau_d' > \tau_d$). Therefore, the simpler *D*-type flip–flop was chosen for this circuit, with the understanding that overall circuit speed was being traded for design simplicity and ultimately circuit yield. Divider circuits utilizing the $1/2\tau_d$ flip–flops are now under investigation at our laboratory.

III. Circuit Design and Operation

Fig. 2 shows a schematic of the entire variable modulo divider circuit. Flip–flops 1 through 3 operate as a synchronous counter and will perform either the divide-by-5 or the divide-by-6 function as controlled by the mode-select inputs. With either mode-select line high, the divide-by-5 mode is selected. With both select lines low, the divide-by-6 mode is selected. When the input is applied through the prescaler circuit, the input frequency is divided by 2, and the output frequency of flip–flop 3 will be $f/10$ or $f/12$ (where f is the input frequency). Exclusive OR circuitry allows the polarity of the output signal to be selected, and a buffer is provided to drive external circuitry. Flip–flops 4 through 6 operate as a ripple type divide-by-8, and control the operation of the divide-by-5,-6 circuitry along with the mode-select lines. With this control, the divide-by-40 function is realized by eight cycles of the divide-by-5 function, and the divide-by-41 function is realized with 7 cycles of the divide-by-5 and 1 cycle of the divide-by-6 function. The divide-by-80 and -82 functions are realized in the same manner with the use of the prescaler. The clear line controlling flip–flops 4 through 6 must be activated when operating in the divide-by-5, -6, -10, or -12 modes to override the control of the first three stages.

Fig. 3 depicts a photomicrograph of an actual circuit. The large horizontal devices between the bonding pads around the periphery of the circuit are 360-μm wide interdigitated FET's connected as source followers to drive the signals off chip. The smaller vertical devices between the

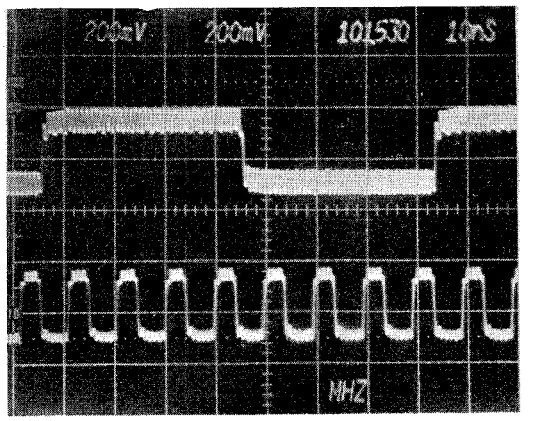

Fig. 4. Oscillogram of circuit outputs of SDFL divider wafer probe. Upper trace: divide-by-80 output. Lower trace: divide-by-10 output. $F_{in} = 1.015$ GHz.

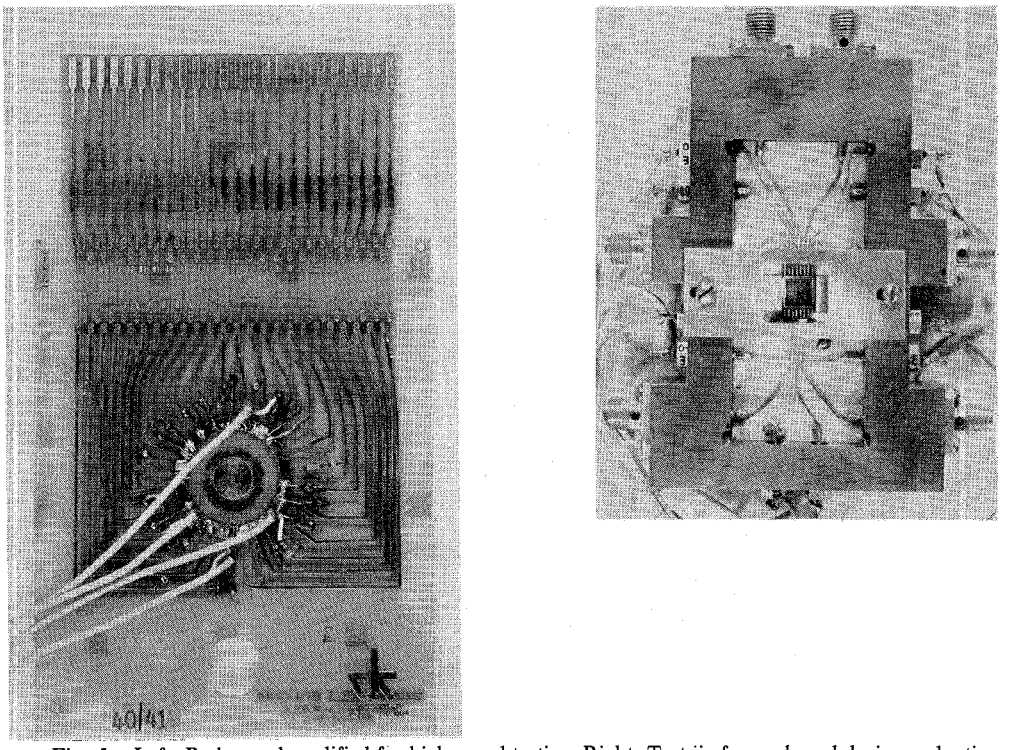

Fig. 5. Left: Probe card modified for high-speed testing. Right: Test jig for packaged device evaluation.

bonding pads in the upper left are on-chip 50-Ω resistors to terminate the clock input signal at either the prescaler input, or the direct input to the divide-by-5, -6 stage.

The variable modulo divider circuit contains 60 gates. The overall size of the chip is 1.35 mm × 0.9 mm.

IV. Circuit Performance

Fig. 4 is an oscillogram of the circuit output in the divide-by-80 mode (top trace), and the divide-by-10 mode (lower trace). This oscillogram was taken at wafer probe with an input clock frequency of 1.015 GHz. The probe card used to perform the measurements is shown at the left side of Fig. 5. It is a standard probe card, which has been modified for high-frequency performance. Miniature 50-Ω coaxial cables are connected directly to the probe card, as close as possible to the actual probes. The traces on the printed circuit board are cut wherever a 50-Ω cable is connected. Bypass capacitors are soldered directly on the probe card for all of the power supply lines.

High-frequency performance can be obtained from this modified probe card because of the nature of the circuit, and the clock signal that is introduced to the circuit through the probe card. This input clock signal is sinusoidal because of the difficulty involved in generating pulse trains of sufficient amplitude at frequencies above 1 GHz. Therefore, at any given frequency, the distortion arising from termination mismatch will affect only the amplitude and phase of the input signal (i.e., there is no ringing). Since the input phase is not important to the divider circuit, the only remaining concern is to ensure that there is sufficient amplitude at the input. This can be easily accommodated, if a signal generator with sufficient power output is used.

The output signals all have fundamental frequencies more than two octaves lower than the input signal. This makes them far less prone to the effects of mismatched impedances. The output signals shown in Fig. 4 do exhibit

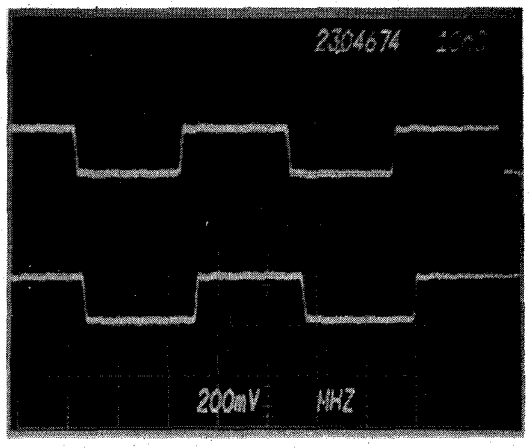

Fig. 6. Oscillogram of packaged device outputs showing the divide-by-80 and divide-by-82 outputs for an input frequency of 1.84 GHz. The average propagation delay per gate is 109 ps. The total power dissipation is 94.5 mW (1.58 mW/gate).

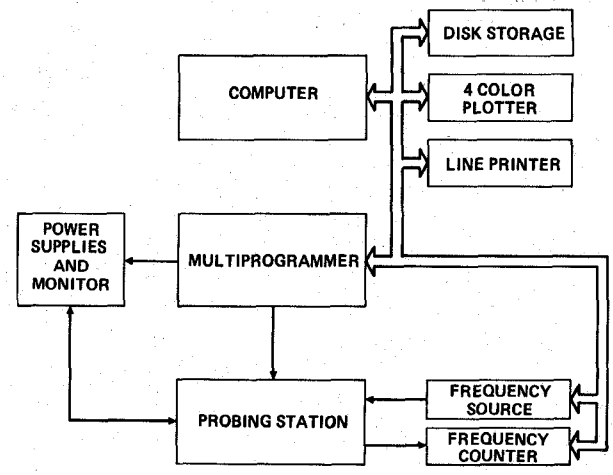

Fig. 7. Test setup for automatic dc and RF circuit characterization.

some hint of ringing, and a discernable amount of clock feedthrough.

Packaging the device in a 16-lead flat package allows the samples to be evaluated in the test jig shown on the right of Fig. 5. This jig has 50-Ω microstrip transmission lines on alumina substrates leading directly to the edge of the flat package. A clamp secures the leads of the flat package to the substrates. This allows for easy interchangability of the flat packages without soldering. Chip-bypass capacitors are provided on the underside of the substrates through wrap around lines. Since the capacitors are closer to the device under test, and the lengths of uncontrolled impedances are shorter than those of the modified probe card, superior high-frequency performance is to be expected with the test jig.

Such results are shown in Fig. 6, which is an oscillogram of the outputs of a packaged device, operating in the $f/80$ and $f/82$ modes. This device was operated with a clock frequency of 1.84 GHz, which represents the best result obtained thus far, for this circuit. This frequency corresponds to an average τ_d of 109 ps/gate, a very low propagation delay for a circuit with fan out larger than one employing 1-μm gate FET's.

The power required at this frequency was 94.5 mW, which corresponds to an average power dissipation of 1.58 mW/gate. (This does not include power consumption by the interdigitated source follower FET's.) Although this power consumption is already quite low, it can be made even lower if the device operates at a frequency below the absolute maximum of which it is capable. This is exemplified by another data point from the same device, operating at 1.80 GHz, consuming 84 mW of power, or an equivalent of 1.45 mW/gate. This represents operation at 9 percent lower power dissipation for a 2.5-percent reduction in speed.

V. Circuit Yield

Comparing the sharp waveforms of the packaged device shown in Fig. 6 to those of the wafer probed device in Fig. 4 clearly demonstrates the advantage of using packaged devices for high-speed characterization. However, automated testing is much easier to implement with probe cards, which can be used to assess circuit performance up to 2.5 GHz. With 128 divider circuits to be evaluated per wafer, the convenience of wafer probing cannot be overlooked. Fig. 7 shows a block diagram of the test system used for dc and RF characterization of these circuits. A Hewlett-Packard 9800 series computer controls the dc bias

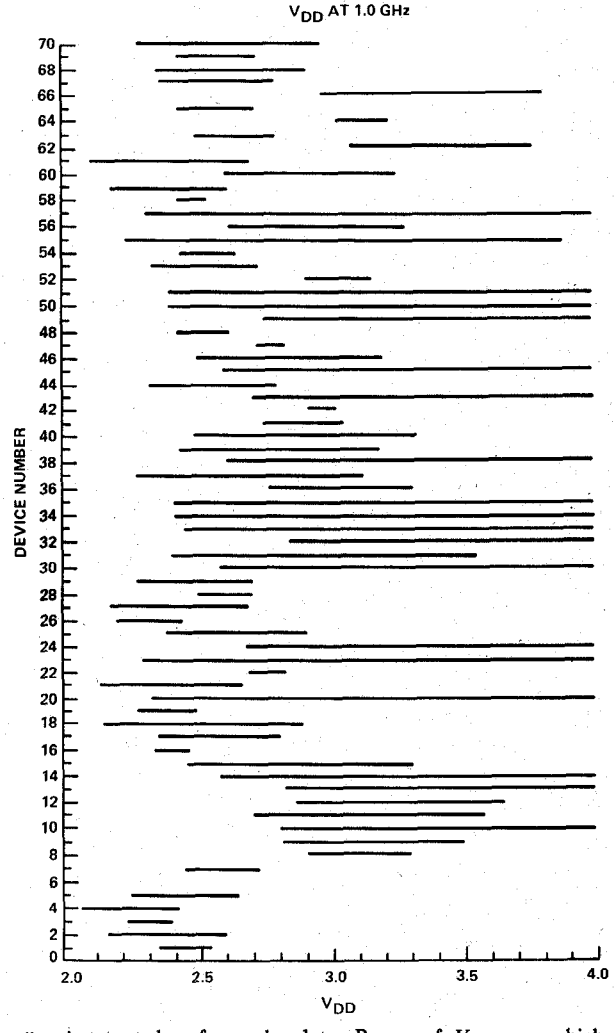

Fig. 8. Automated wafer probe data: Range of V_{OD} over which the circuit operates at 1 GHz for example, of the 128 circuits on a wafer.

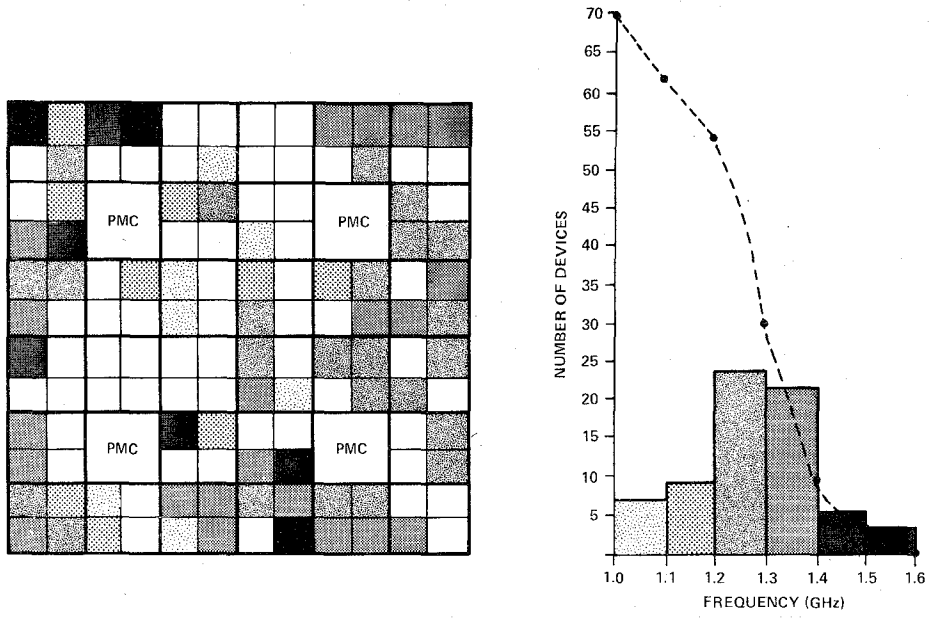

Fig. 9. Wafer map and histogram of circuits operating in several frequency intervals.

voltages applied to the circuit and monitors the current supplied through a multiprogrammer. The output frequency is measured and fed to the computer by a high-frequency counter. The accompanying peripherals store and output the acquired data. The following figures represent the data acquired from the automatic test system in various formats. All of the following data is from wafer probed devices operating in the $f/40$ and $f/41$ modes.

In Fig. 8 we see the range of one supply voltage for which the divider circuits on one wafer will operate at a fixed frequency. These data are useful in determining the best fixed voltage to use over a large number of circuits. Fig. 9 presents additional information that is obtained from wafer probing on the automatic system. On the left is a wafer map which shows the location and maximum operating frequency of all the working circuits on the wafer. These data would be helpful in identifying process anomalies, as well as for predicting yields of larger circuits. The boxes labeled PMC represent drop-in chips with process monitoring circuits not included in this test [10]. On the right side on Fig. 8 is a histogram of the number of working devices versus their maximum frequency of operation. The dotted curve above integrates the histogram. It shows a total of 70 of the 128 devices on this wafer operating at or above 1 GHz. This number represents a yield of 54.7 percent.

The high yield obtained for one wafer has been repeatedly obtained for a number of wafers. In Fig. 10, the yield of devices working at or above 1 GHz on six different wafers are shown. The average yield for all six wafers is > 50 percent. This figure is quite high, and it reinforces the growing consensus that the digital GaAs IC technology is indeed reaching maturity.

Several issues remain. Sensitivity of the GaAs circuits to supply voltage variation must be further explored. Operation over wide temperature ranges must also be explored since FET threshold voltage are sensitive to temperature

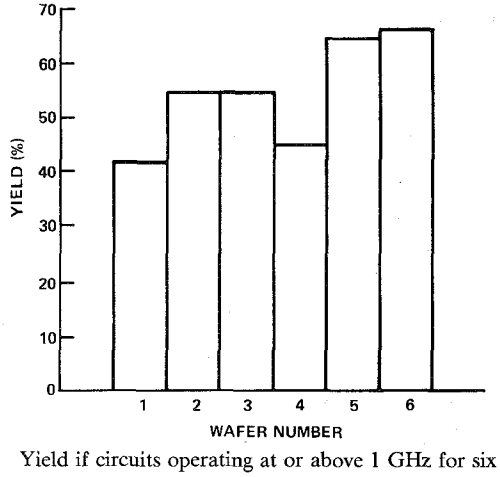

Fig. 10. Yield if circuits operating at or above 1 GHz for six wafers.

[11]. Assuring operation of the circuits over convenient range of supply voltages and a wide temperature range will result in a penalty in terms of yield. Despite these drawbacks, this young technology has margin for improvements. For example, replacing the FET active loads by saturated resistors appears as a very promising improvement in terms of temperature and backgating sensitivity of the circuits [12]. In terms of radiation hardness, recent results indicate great tolerance of digital GaAs circuits not only to total dose of ionizing radiation, but also to radiation transients [13], [14].

VI. Conclusions

In this paper, we have described the technology used to develop a high-speed SDFL divider circuit with multimode frequency division capabilities. This flexibility lends the circuit to various L-band applications. The operation of this circuit was discussed and performance results were presented. The best performance of this circuit was operation with an input clock frequency of 1.84 GHz. This

performance was achieved while consuming only 94.5 mW of power (exclusive of source follower FET power consumption) with even lower power consumption (87 mW) at slightly lower (1.797 GHz) frequencies.

A probe card, modified for high-frequency operation, and a high-speed test jig were described, and the relative merits of each were discussed. Automatic testing of these devices was described, and the test results were presented. The value of the various formats of output data available from the automated test system was shown. These results showed that good yields can be attained consistently from SDFL circuits, using a planar process, at MSI complexity. It was further shown that these high yields can be repeatedly attained over a number of wafers with an average yield of over 50 percent. This figure is quite high, and it reinforces the growing consensus that the digital GaAs IC technology is reaching maturity for full-scale utilization.

ACKNOWLEDGMENT

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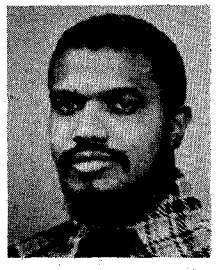

Emory Walton (M'80) received the B.S. degree in electrical engineering from New York University in 1972. He joined Xerox, working on circuit designs for Facsimile systems and electronic imaging terminals. This work began in Rochester, NY and continued in Dallas, TX and El Segundo, CA. In 1978 he joined Rockwell International, Integrated Circuits Section, where he is now involved in the design and test of high-speed GaAs digital IC's.

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Later he held a position of Professor (in Physics) at the University at Rosario, Argentina. Since joining Rockwell International in 1972, he has been engaged in several aspects of semiconductor technology, focusing mainly on the electrical properties of semi-insulating GaAs, the substrate material for most GaAs high-frequency semiconductor devices. More recently he has been involved in the development of a high-speed, low-power planar GaAs digital IC technology with potential for LSI/VLSI applications. His work involved the development and application of testing techniques for process characterization and evaluation. He is now Manager of the GaAs Integrated Circuits Design and Test Section.

Dr. Zucca is a member of the American Physical Society.

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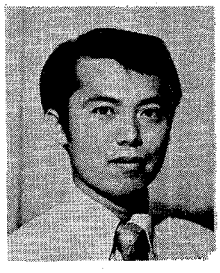

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Mr. Welch is a member of the Electrochemical Society.

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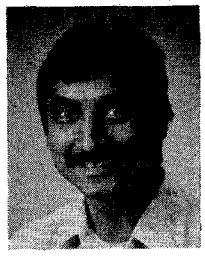

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In 1973 he joined RCA Limited in Montreal, where he designed and developed components for communications satellites. This included waveguide filter multiplexers, diode and GaAs FET mixers and GaAs FET MIC amplifiers, and automatic testing technology. In 1978 he joined Rockwell International, in Anaheim, CA, in the GaAs Device Development group. He is currently working on automatic high-speed test technology development for GaAs Integrated Circuits.